# CSIR-CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE, PILANI (RAJ.)

Date: 24.12.2021

F.No. 4/2-3(2)/2016-Estt.I

### Advt. No. PF-07/2021

## "Online Interview"

CSIR-Central Electronics Engineering Research Institute (CSIR-CEERI) is a premier research Institute in the field of Electronics, set up under the Council of Scientific & Industrial Research (CSIR). The Institute is looking for qualified candidates for the following project staff positions on purely temporary engagements for various ongoing projects in the Institute.

# Online applications are invited from candidates for Engagement of Project Staff.

### **Details of Vacancies & Eligibility**

Post Code	Project No.	Area/Group	Name & Number of Vacancy	Qualifications	Age	Consolidated Emolument per month (fixed)
0801	HCP-0101	Technology Business Development	Project Associate-I  02	Essential: (I) B.E./ B.Tech./ M.Sc. in (Electronics/Electronics & Communication/Computer Science ) or equivalent (II) selected through a process described through any one of the following: (a) Scholars who are selected through National Eligibility Tests- CSIR-UGC NET including lectureship (Assistant Professorship) and GATE. (b) The selection process through National Level examinations conducted by Central Government Departments and their Agencies and Institutions such as DST, DBT, DAE, DOS, DRDO, MHRD, ICAR, ICMR, IIT, IISC, IISER etc.  Desirable: Programming skills and development Experience in 3D models and animation using Blender, Unity 3D, Vuforia, and equivalent tools for AR/VR applications. Skill to develop animations and video editing Or Android app development for AR/VR applications. Skill to develop animations and video editing Or Android app development for AR.	35 Years	₹31,000/- + HRA as per rule

0802	HCP-0101	Technology Business Development	Project Associate-II 02	B.E. / B.Tech/ M.Sc. in (AI/Computer Science/Electronics & Communications/ EEE/CE) or equivalent + 02 Years' of experience in R&D in Industrial and Academic institutions or Science & Technology organizations and scientific activities and services.  OR M.Sc. (Electronics)/B.E./ B.Tech. / (Electronics & Communication/Telecommunicati on/ Electronics & Telecommunication) or equivalent + 02 Years' of experience in relevant filed.  Desirable: M.E./M.Tech.  OR  Possessing any skills given below "Programming skills and development Experience in 3D models and animation using Blender, Unity 3D, Vuforia, and equivalent tools for AR/VR applications. Skill to develop animations and video editing Or Android app development for	35Years	*₹35,000/- + HRA as per rule OR *₹28,000/- + HRA as per rule
0803	GAP-6221	Intelligent Systems Group	Project Junior Research Fellow 01	Android app development for AR/VR applications. Skill to develop animations and video editing Or Android."  Essential:  (I) B.E./ B.Tech./ M.Sc. in (Electronics/Instrumentation/ Instrumentation and Control Systems/Electrical Engineering/EEE/CS/CE) or equivalent (II) selected through a process described through any one of the following:  (a) Scholars who are selected through National Eligibility Tests-CSIR-UGC NET including lectureship (Assistant Professorship) and GATE.  (b) The selection process through National Level examinations conducted by Central Government Departments and their Agencies and Institutions such as DST, DBT, DAE, DOS, DRDO,	35 Years	₹31,000/- + HRA as per rule

0804	GAP-3330	Vacuum	Project	MHRD, ICAR, ICMR, IIT, IISC, IISER etc.  Desirable: M.E./M.Tech. in (Electronics/Instrumentation/ Instrumentation and Control Systems/Electrical Engineering/EEE/Electronics & Communication/Computer Science or equivalent.  OR  Circuit and PCB Design on various tools, experience to work with different microcontrollers, Front and Backend development for Web and Android App. Languages: C, C++, Python, Java, CSS, HTML etc. (as special skills)  (I) B.E./ B.Tech./ M.Sc. in (Nano	35 Years	,
		Electron Devices Development Group	Junior Research Fellow 01	Technology/Chemical Technology/ Material Science/Chemistry/ECE) or equivalent (II) selected through a process described through any one of the following: (a) Scholars who are selected through National Eligibility Tests- CSIR-UGC NET including lectureship (Assistant Professorship) and GATE. (b) The selection process through National Level examinations conducted by Central Government Departments and their Agencies and Institutions such as DST, DBT, DAE, DOS, DRDO, MHRD, ICAR, ICMR, IIT, IISC, IISER etc.		as per rule
0805	GAP-3242	Semiconductor Device Fabrication Group	Project Associate-II	(I)M.Sc. in (Physics/Electronics)/B.E. / B.Tech. (Optoelectronics/ Applied Physics/LASER/Nano Technology/Electronics/ Electronics & Communication/Material Science) or equivalent. (II) 02 Years' of experience in R&D in Industrial and Academic institutions or Science & Technology organizations and scientific activities and services. (III) selected through a process described through any one of the	35 Years	₹35,000/- + HRA as per rule

				following: (a) Scholars who are selected through National Eligibility Tests-CSIR-UGC NET including lectureship (Assistant Professorship) and GATE. (b) The selection process through National Level examinations		
				conducted by Central Government Departments and their Agencies and Institutions such as DST, DBT, DAE, DOS, DRDO, MHRD, ICAR, ICMR, IIT, IISC, IISER etc.		
0806	HCP-0034	Semiconductor Device Design Group	Project Associate-II	Essential: B.E./B.Tech./M.Sc.(Electronics/ Instruments/Nanotechnology/ MEMS) or equivalent + 02 Years' of experience in R&D in Industrial and Academic institutions or Science & Technology organizations and scientific activities and services. Desirable: M.Tech.(Electronics/Instruments/ Nanotechnology/MEMS) or equivalent	35 Years	*₹35,000/- + HRA as per rule OR *₹28,000/- + HRA as per rule
0807	GAP-3415	Skill Development Unit	Project Associate-I	BE / B.Tech./M.Sc. in (Electronics & Communication Engineering/ Electronics & Instrumentation/CE/CSE) or equivalent	35 Years	₹25,000/- + HRA as per rule
0808	NWP-100	Skill Development Unit	Project Associate-I 01	BE / B.Tech. in (Electronics & Communication Engineering/ Electronics & Instrumentation/CSE) or equivalent (Specialisation in VLSI/Microelectronics will be preferred)	35 Years	#₹31,000/- + HRA as per rule OR #₹25,000/- + HRA as per rule
0809	GAP-3412	Skill Development Unit	Financial Executive Assistant  01 (Position is for PCI-PIU at MeitY, New Delhi)	B.Sc./B.Com/B.A./BBA/BCA or equivalent with minimum 55% marks	35 Years	as per rule
0810	GAP-3412	Skill Development Unit	Administrative Executive Assistant 01 (Position is for PCI-PIU at MeitY, New Delhi)	B.Sc./B.Com/B.A./BBA/BCA or equivalent with minimum 55% marks	35 Years	₹20,000/- + HRA as per rule

0811	HCP-0026	Intelligent	Project	Essential:	35	*₹35,000/ <b>-</b> +
0011	1101 0020	Systems	Associate-II	BE / B.Tech. in (Electronics &	Years	HRA as per rule
		Group	71330Clate-11	Communication	1 cars	Titer as per rule
		Group	01	Engineering/Computer		OR
			01	Science/Information		*₹28,000/- +
				Technology/Electrical		HRA as per rule
				Engineering) or equivalent		That as per raic
				with 02 years experience		
				Desirable:		
				ME / M.Tech. in (Computer		
				Science/Embedded		
				System/Data Science)		
				OR		
				Machine Vision, Data Fusion, Data		
				Modelling, Machine learning, Deep Learning Languages: C, C++, Python,		
				Java, CSS, HTML (as special skills)		
0812	GAP-	Intelligent	Project	Essential:	35	₹31,000/- +
	3137	Systems	Junior	(I) BE / B.Tech. in	Years	HRA as per rule
		Group	Research	(Electronics &		
			Fellow	Communication		
				Engineering/Computer		
			02	Science/Information		
				Technology/Electrical		
				Engineering) or equivalent		
				(II) selected through a process		
				described through any one of the following:		
				(a) Scholars who are selected		
				through National Eligibility Tests-		
				CSIR-UGC NET including		
				lectureship (Assistant		
				Professorship) and GATE.  (b) The selection process through		
				National Level examinations		
				conducted by Central Government		
				Departments and their Agencies		
				and Institutions such as DST,		
				DBT, DAE, DOS, DRDO,		
				MHRD, ICAR, ICMR, IIT, IISC, IISER etc.		
				Desirable:		
				M.E./M.Tech. in		
				(Electronics/Instrumentation/		
				Instrumentation and Control		
				Systems/Electrical		
				Engineering/EEE/CS/CE) or		
				equivalent. OR		
				Circuit and PCB Design on various		
				tools, experience to work with		
				different microcontrollers, Front and		
				Backend development for Web and Android App.		
				Languages: C, C++, Python, Java,		
				CSS, HTML (as special skills)		

#	(1) ₹31,000/- + HRA to Scholars who are selected through-
	(a) National Eligibility Test- CSIR-UGC NET including lectureship(Assistant Professorship) or GATE or
	(b) A selection process through National level examinations conducted by Central Government
	Departments and their Agencies and Institutions.
	(ii) ₹25,000/- + HRA for others who do not fall under (i) above.
*	(i) ₹35,000/- + HRA to Scholars who are selected through-
	(a) National Eligibility Test- CSIR-UGC NET including lectureship (Assistant Professorship) or GATE or
	(b) A selection process through National level examinations conducted by Central Government
	Departments and their Agencies and Institutions.
	(ii) ₹28,000/- + HRA for others who do not fall under (i) above

Note: If any candidate wishes to apply for more than one position, then such candidates have to apply separately.

Interested candidates fulfilling the above qualifications must apply through project staff recruitment portal of CSIR-CEERI. Link for online portal is available on CEERI website. A print out of the Application Form must be taken by the candidate after successful submission of the form. The shortlisted candidates will be informed through E-mail/Institute website along with the date and time for interview. Candidates are requested to frequently browse the institute website and registered Email. The eligible candidates must appear for interviews through "Microsoft Teams" (MS Teams). Candidates will be allowed as a Guest in MS Team, for which the link will be send to your registered email. The selected candidates are expected to join immediately upon selection and bring with them all ORIGINAL TESTIMONIALS including marksheets and certificates and also a passport size photograph at the time of joining, failing which their offer of engagement can be withdrawn.

#### The last date & time for applying applications is 31.12.2021 till 05:00 PM.

For recruitment queries:
Sh. K.R. Singh
Section Officer

For technical queries:
Sh. Arvind Kumar Khandelwal
Network Management Cell

CSIR-CEERI, Pilani CSIR-CEERI, Pilani

Email: <a href="mailto:arvindkumar@ceeri.res.in">arvindkumar@ceeri.res.in</a>
Phone: 01596 – 252275

Email: <a href="mailto:arvindkumar@ceeri.res.in">arvindkumar@ceeri.res.in</a>
Phone: 01596 – 252282

### **Other Conditions:**

- 1. Candidates who have already served CSIR-CEERI or any other lab/ institute of CSIR as Project Staff such as Project Assistant/ Project Fellow/ JRF (in contract R&D Projects)/ SRF (in contract R&D Projects)/ Research Associate/FEA/AEA etc. for a total period of 5 years or more are not eligible for these engagements. The candidates who have served for a period less than 5 years will have tenure up to remaining period till completion of five years.
- 2. Tenure of engagement: Six months initially or co-terminus with the present project or till such time the job to be performed by Project Staff in the project exists, whichever is earlier. The tenure may be extended in steps of six months for the duration of Project based on satisfactory performance. The total tenure as Research Associate-I, Project Associate-I/II, JRF/SRF/FEA/AEA etc. shall not exceed 5 years in any case. The total tenure of five years shall be calculated as per periods spent on one Project and/ or different Projects taken together in CSIR-CEERI, Pilani and/ or any other Laboratory/ Institute of CSIR as RA, Project Assistant, and Project Associate Level II/III etc. or as any other designation of equal status.

- 3. The date for determining the upper age limit, essential educational qualifications and/or experience shall be the last date of submission of online application.
- 4. The engagement of Project Assistant, Project Associate- I/II, SPA, SRF, JRF, FEA, AEA etc. will be made on behalf of the Sponsor of the Projects. These are not CSIR-CEERI/CSIR positions and will not confer any right on the incumbent to claim, implicit or explicit, on any post in CSIR-CEERI/CSIR.
- 5. Candidates shall upload scanned copies of following documents on Project Staff Recruitment Portal of CSIR-CEERI:-
  - (a) Candidates shall upload scanned copies of following academic certificates while applying for project staff positions:-
    - (i)SSLC/10<sup>th</sup>
    - (ii) HSC/Senior Secondary/Intermediate/12<sup>th</sup>
    - (iii)Graduation Degree (B.A./B.Com./BBA/B.Sc. /B.E. /B.Tech. etc.)
    - (iv)Post Graduation (M.Sc./M.E./M.Tech./MS etc.)

Educational Qualification Certificate as mentioned in the advertisement essential qualification / Semester Mark sheet or Final Mark sheet is compulsory. Along with this, Degree Award Certificate or Provisional Award Certificate. Percentage or CGPA/DGPA should be clearly displayed on any one of the certificate. If certificate doesn't have proper percentage / CGPA /DGPA/Grade then the application may not be considered. The candidate must ensure to provide proper certificates to ensure their eligibility for the positions they are applying for.

- (b) Date of Birth Proof (Any valid certificate having DoB such as SSLC, HSC, DoB Certificate, etc)
- (c) Category certificate (in case of SC/ST/OBC/PWD/EWS candidates)
- (d) NET/GATE/Any other equivalent exam qualification certificate (If applicable)
- (e) Experience certificate (Mandatory for the posts where experience is essential qualification)
- (f) Other certificates (If applicable)
- 6. **Reservation:** As regards reservation, if all things are equal, SC/ST/OBC/PWD/EWS candidates may be given preference over General candidates so as to ensure their representation.
- 7. Relaxation in age limit for SC/ST/OBC/PH and women shall be 5 years.
- 8. If it is found at any stage of the recruitment process or thereafter that the candidates do not fulfil the eligibility criteria, their candidature shall be cancelled without assigning any reason. Further, the decision of CSIR-CEERI in regard to the selection process will be final and binding to all concerned. No correspondence in this regard will be entertained by the Institute.
- 9. Received applications will be screened by duly constituted Standing Screening Committee. The Screening Committee may fix different set of criteria to short-list the candidates as per the project requirement. The Screening Committee will screen all applications received for the specified project and recommend eligible candidates will be called for online interview. In case of false information received through online application, the competent authority will cancel the candidature of the applicant and debar for attending the interview in future.
- 10. Eligible applicants may be called for interview through online and Interview letter will be sent him/her through e-mail intimating the date & time of Interview, link/reference of online mode, terms & conditions, if any. The candidate will be allowed to join only after verification of original certificates and other information found correct.
- 11. Based on the performance of the candidates and availability of suitable candidates, Selection Committee may also recommend Panels for future engagement in different projects as and when need arises. The engagement process will be complete after the joining of the candidates.

- 12. CSIR-CEERI reserves the right to cancel or withdraw the Offer of engagement in case of any discrepancy found, in the candidature of any empanelled candidate at any stage.
- 13. The number of positions may be increased or decreased as per the requirements.
- 14. Other terms & conditions will be governed as per guidelines issued by the funding agency/ CSIR/ CEERI for the engagement of above Project Staff as amended from time to time.

**ADMINISTRATIVE OFFICER**