National Institute of Technology Goa

Institution of National Importance under MHRD, Govt. of India)

Department of Electrical and Electronics Engineering

Advt. No.: NITG/EEE/ADVT/2022/ 002, Dated: 16th August 2022

Advertisement for the Position of Junior Research Fellow under the Project DST/SERB/EEQ/2021/000294

Applications are invited from interested and highly motivated candidates for the post of Junior Research Fellow (JRF) to work on the R&D project titled **"Development of Metaheuristic Algorithms based Maximum Power Point Tracking Controllers for various Grid-Connected/Stand-Alone PV System to Enhance the Maximum Power Generation Capability",** has been sanctioned by **Science and Engineering Research Board (SERB), Dept. of Science and Technology (DST), Govt. of India**. JRF will be appointed initially for one year (on contract) and his/her services will be extended for subsequent year(s) based on the performance review. The position is co-terminus with the project.

Name of Project Investigator : Dr. Suresh Mikkili

Department : Electrical and Electronics Engineering

Duration of the project : 3 Years (2022-2025)

S No.	Position	Basic Qualification	Desirable knowledge areas	Duration	Consolidated Salary	Number of Positions
1	JRF	**M.Tech.**/M.E. in Electrical and Electronics/ Electrical Engineering and B. Tech/B.E. in Electrical and Electronics/ Electrical Engineering	MATLAB, Digital Signal processor (DSP), Grid-tied PV System, and Optimization Techniques.	Initially for the period of one year which may be extended upto maximum of 3 years	Rs. 33,480/- (Per month upto 2 years) Rs. 37,800 (Per month for 3rd year)	01 (One)

Eligibility for JRF:

1. **M.Tech**./M.E. in Electrical Engineering / Electrical and Electronics Engineering with at-least 6.5 CGPA or 60 percent marks in aggregate from a recognized technical institute or university as a full time program.
2. B. Tech/B.E. in Electrical Engineering / Electrical and Electronics Engineering with at-least 6.5 CGPA or 60 percent marks in aggregate from a recognized technical institute or university as a full time program.
3. SC/ST/OBC/EWS/WOMEN/PWD candidates will get relaxation as per Government of India Rules and Regulations.

Note:

- **Candidate selected for this position will have the opportunity to register for Ph. D. program in NIT Goa provided they satisfy the Institute eligibility criteria for the same.**
- The candidate should have qualified GATE in the past to register for Ph.D. program
- Decision of the project selection committee will be final in all respects.

Desirable Qualification for JRF:

A strong knowledge of MATLAB-Simulink is highly desirable. Additionally knowledge in Grid-tied PV System, MPP Techniques, Optimization Techniques, Multi-level Inverters and DSP Controller programming would be appreciated.

Objective of the Project

- To develop 5 KW PV array configurations such as Series-Parallel (SP), Bridge-Link (BL), Honeycomb (HC), and Total-Cross-Tied (TCT) configurations. The performance of these architectures should be tested under various partial shading conditions.
- For all the above developed configurations, boost converter should be integrated along with the PV MPPT controller for harvesting maximum power under partial shading conditions.
- To track the global maximum power from SP, BL, HC, and TCT configurations of PV modules, metaheuristic algorithms based MPPT techniques need to be developed for better accuracy and speed to get global best.
- The performance of SP, BL, HC, and TCT configured PV MPPT systems with various optimization MPPT techniques need to be compared for selecting the best configuration with optimized MPPT controller.
- To develop proposed TCT configured SMA Algorithm based PV MPPT System and the performance will be compared with other existing MPPT techniques such as Particle Swarm Optimization (PSO), Artificial Bee Colony (ABC), Ant Colony Optimization (ACO), and Frog Leaping Algorithm (FLA) etc.
- The proposed TCT configured SMA Algorithm based PV MPPT system need to be grid-integrated by employing the various types of multi-level inverters and the performance is verified under partial shading conditions.
- Under PSCs, the power quality issues need to be checked, whether they meet the requirement of IEEE grid standards and codes or not.

Important Instructions:

1. Candidate selected for this position will have an opportunity to register for Ph. D. program in NIT Goa provided they satisfy the Institute eligibility criteria for the same.
2. Candidate possessing the requisite qualification and experience should apply; in the attached format along with their updated CV latest by **05th September 2022**.The applicant will be responsible for the authenticity of information, other documents and photographs submitted.
3. Mere, possessing the prescribed qualification does not ensure that the candidate would be called for Interview. The Candidates will be shortlisted on the basis of merit and need of the project.
4. Applicants in employment (private, government or any other organization) are required to submit a "**No Objection Certificate**" from the employer at the time of interview.
5. Duly filled and signed scan copy of Application Form along with the scan copies of mark sheets/documents must be sent to Dr. Suresh Mikkili (PI), **through e-mail**, at: mikkili.suresh@nitgoa.ac.in, with subject line "**Application for the post of JRF in the Department of EEE under DST/SERB/EEQ/2021/000294"**

6. The Shortlisted Candidates will be informed by e-mail (apart from website) along with the date and time of the written test/interview. No other letter will be sent to the correspondence address. So, the candidates are advised to check their email regularly.
7. Shortlisted candidates have to present themselves for the interview on the interview date with updated CV, application form, original and attested photocopies of mark sheets/certificates in support of their academic qualifications.
8. No TA/DA shall be paid to candidates for attending the Interview and/or joining the position.
9. The appointment is for time bound project and the candidate is required to work dedicatedly for the successful completion of the project. Selected candidate has to join immediately.
10. Incomplete application forms and forms received after due date will be summarily rejected.
11. All the Terms and Conditions for this recruitment will be as per guidelines of DST SERB, Govt. of India.

Application Process

Application form (as given below) giving all the details and attested copies of certificates, supporting documents and experience should reach the undersigned latest by **05th September 2022**. Candidates who are already employed should produce relieving certificate from their employers, if selected. The written test/interview will be conducted for all the eligible candidates. The applicants need to bring all the original documents for verification during written test/interview. The list of shortlisted candidates will be posted in the NIT Goa website (www.nitgoa.ac.in) along with the date and time of the written test/interview.

Address for Correspondence

Dr. Suresh Mikkili,
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National Institute of Technology Goa,
Farmagudi, Ponda, 403401, Goa- India.
Telephone: +917588133009, 0832-2404214
Email: mikkili.suresh@nitgoa.ac.in
Website: www.nitgoa.ac.in

NOTE: The envelope containing the application should be super scribed as "**Application for the post of JRF in the Department of EEE under DST/SERB/EEQ/2021/000294"**

Dr. Suresh Mikkili

National Institute of Technology Goa

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Department of Electrical and Electronics Engineering

Application for the post of JRF in the Dept. of EEE under DST/SERB/EEQ/2021/000294

Title of Project: Development of Metaheuristic Algorithms based Maximum Power Point Tracking Controllers for various Grid-Connected/Stand-Alone PV System to Enhance the Maximum Power Generation Capability

1. Post Applied for : Junior Research Fellow (JRF)
2. Name of the Candidate (BLOCKL ETTER):_____
3. Father's Name (BLOCK LETTER): _____
4. Mother's Name (BLOCK LETTER): _____
5. (a) Date of Birth: (DD/MM/YYYY)_____

Paste here a recent Passport size Photograph

(b) Sex (Male/Female/Other):_____

(c) Marital Status (Married/Single):_____

(d) Category (SC/ST/OBC/PWD/GEN):_____

6. Previous Research experience: (use additional sheet if required)_____
7. Publication(s), if any: (use additional sheet if required)_____
8. GATE : Qualified (Yes/No): Score:_____Rank:_____

Specialization: _____Year: _____

9. Academic Qualification: (Starting from Standard 10 or equivalent Examination)

Name of the Exam Passed	Name of the School/College/Institute/ University	Year of Passing	Discipline/ Specialization	Percentage of Marks/ CGPA

10. (a) Address for Communication: (BLOCK LETTER)

(b) Contact No. (Mobile)

(c) E-mail ID :

11. Contact Details of two referees:

	Referee -I	Referee- II
Name :		
Designation :		
Organization:		
Office Address :		
Office Phone Number:		
Email ID:		

12. Experience details:

I do here by declare that the information furnished in this application is true to the best of my knowledge and belief. If selected, I promise to abide by the rules and regulations of the Institute.

Date:

Place: Signature of the candidate

Note:-Additional A4 sheets may be included if provided space is insufficient.