Indian Institute of Technology Ropar
Department of Electrical Engineering
IIT Ropar, Rupnagar, Punjab, India - 140001

Advertisement for JRF in MeitY sponsored Project [SMDP-C2S]

Applications are invited for junior research fellow (JRF) positions (three nos.) in the Department of Electrical Engineering, IIT Ropar under the project titled "**ASIC and package design of ultra small atomic clock"**. Eligible and interested candidates are requested to apply by the deadline (as per the institute deadline of PhD admission).

Essential qualifications: As per the JRF admission criteria of the funding agency.

Desired qualifications: Strong fundamentals in the area of CMOS analog integrated circuit design. Experience in electronic circuit and PCB design, soldering, testing, characterization and electronic system prototype development will be an added advantage.

Duration: The duration of the project is thirty-six (36) months.

Salary: A consolidated salary of **Rs. 37000/- per month** will be provided as per the institute norms.

The interested candidates must apply in the regular PhD admission process of IIT Ropar [https://www.iitrpr.ac.in/academic/phd] and choose the option "**Microelectronics and VLSI Design**" as the first preference. The selected candidate will be registered for the PhD degree.

The interview for this position will be held along with the PhD admission interviews of the Microelectronics and VLSI Design group of the Electrical Engineering Department of IIT Ropar. The candidates should also visit the admissions website periodically for the latest updates on the PhD admission process.

For any further information, please contact the co-principal investigators:

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