



# राष्ट्रीय प्रौद्योगिकी संस्थान दिल्ली

## NATIONAL INSTITUTE OF TECHNOLOGY DELHI

(शिक्षा मंत्रालय, भारत सरकार के अधीन एक स्वायत्त संस्थान)

(An autonomous Institute under the aegis of Ministry of Education (Shiksha Mantralaya), Govt. of India)

Plot No. FA7, Zone P1, GT Karnal Road, Delhi-110036, INDIA

दूरभाष/Tele: +9111-33861000, 1001, 1005 फैक्स/ Fax: +9111-27787503,

वेबसाइट/Website: [www.nitdelhi.ac.in](http://www.nitdelhi.ac.in)

Date: 05.04.2024

### **ADVERTISEMENT FOR JUNIOR RESEARCH FELLOW (JRF) under the**

#### **Chips to Startup (C2S) Programme**

**Last date for Application: 05.05.2024**

Applications in the prescribed formats are invited from highly motivated and dynamic eligible candidates for one position of **Junior Research Fellow (JRF)** in the following Ministry of Electronics & Information Technology (MeitY), R&D in Electronics Group (Microelectronics Development Division), Govt. of India sponsored research project:

**Project Title:** A Novel power-on pilot IC for ultra-low power wireless IoT devices

**Funding Agency:** Ministry of Electronics & Information Technology (MeitY)

**Project Duration:** Three (03) years or position is coterminous with the project.

**Chief Investigator & Co-Chief Investigator (CI & Co-CI):**

Dr. Baljit Kaur & Dr. D. Vaithyanathan

Department of Electronics and Communication Engineering, National Institute of Technology Delhi

**The minimum essential and desirable qualifications for the project posts are as follows:**

Name of the Position	Junior Research Fellow (JRF), One (01)
Essential Qualifications	<ul style="list-style-type: none"><li>• Candidates with a Bachelor's degree in Engineering/Technology in Electronics and Communication Engineering or Electrical and Electronics Engineering or Computer Science and Engineering or other relevant discipline.</li></ul> and <ul style="list-style-type: none"><li>• Master's degree in Engineering/Technology in the fields of VLSI Design/Microelectronics/Embedded Design/ECE or other relevant discipline, with a minimum of 60% aggregate marks (or) CGPA of 6.5/10 in UG or PG for JRF under GEN/EWS/OBC category and 55% aggregate marks or equivalent CGPA of 6.0 for SC/ST candidates.</li></ul>
Duration	03 Years  The initial appointment for one (01) year which can be extended up to the completion of the project, purely based on satisfactory performance. The position is co-terminus with the project.

Emoluments	Rs. 37,000/- (for the first 2 years) and Rs. 42,000/- pm (for the 3rd year) plus House Rent Allowance (HRA) as per the norms of GoI
Desirable Qualification/ Skills:	Knowledge in Verilog HDL, Cadence Tool, Siemens EDA Tools (Mentor graphics), Synopsys TCAD etc.
Nature of appointment	It will be governed by the administrative rules and conditions of Research & Consultancy NIT Delhi / Institute norms.
Other Benefits	<b>The selected candidate shall be encouraged to register for Ph.D. at NIT Delhi as per institute norms.</b>
Age Limit	<b>Not exceeding 30 years (for JRF) as of the closing date of the application. Age relaxation as per GoI norms.</b>

#### HOW TO APPLY:

1. Eligible and Interested candidates can apply as per the below instructions:
  - (i) Fill out the Google form [https://docs.google.com/forms/d/1y4IGX\\_n5II49Bh1Ohng6iiS4WrwR2nP\\_3Z35m5LnR10/prefill](https://docs.google.com/forms/d/1y4IGX_n5II49Bh1Ohng6iiS4WrwR2nP_3Z35m5LnR10/prefill) and attach the application as per the attached format in Annexure - I along with the self-attested copies of the relevant certificates/documents.
  - (ii) No other form of application is accepted.
  - (iii) **PLEASE DO NOT SEND ANY HARD COPY.**
  - (iv) **The last date of registration and application along with the documents is 05.05.2024.**

#### INSTRUCTIONS:

1. No TA/DA is permissible for appearing in the interview and joining in case of selection.
2. The selected candidate shall be encouraged to apply and register for Ph.D. Programme of the Institute as per the prevailing norms. Preference may be given to candidates willing to pursue a Ph.D. degree at NIT Delhi.
3. The appointment will be purely a project-based temporary position as per the MeitY norms.
4. Candidate shall bring along with them the original degree(s)/certificate(s) and experience certificate(s) at the time of interview for verification.
5. Candidates will be informed by e-mail about the interview date. So, candidate must provide valid e-mail IDs in their applications.
6. The applicant will be responsible for the authenticity of the information, other documents and photographs submitted.
7. The selected candidate will have to join the assignment immediately upon receipt of the offer letter.

8. The appointed candidate will be placed at the National Institute of Technology Delhi and the appointment will be made purely temporarily initially for one year and can be extended up to the completion of the project based on the performance. The contract will also include a one-month notice period wherein if the candidate selected wants to discontinue the project, he/she will have to inform the CI/Co-CI one month in advance and in case the CI/Co-CI is not satisfied with the performance of the candidate, he will need to inform the candidate one month before termination of contract.
9. Any queries related to the above post must be addressed to: Dr. D.Vaithyanathan, Email: [dvaithyanathan@nitdelhi.ac.in](mailto:dvaithyanathan@nitdelhi.ac.in).

**Dr. D.Vaithyanathan**

Assistant Professor

Department of Electronics and Communication Engineering

National Institute of Technology Delhi

Plot No. FA7, Zone, P1, GT Karnal Rd, Delhi, 110036

Email: [dvaithyanathan@nitdelhi.ac.in](mailto:dvaithyanathan@nitdelhi.ac.in)

Phone No.: 011-1133861154/ +91-9865806300

Copy to:

1. PS to Director (for kind information).
2. Dean (R&C).
3. Head of Department, ECE.
4. Office of Registrar.
5. Head, Computer Centre (for displaying the advertisement on the Institute website).
6. Office Copy/Project File.
7. Institute Notice Boards.



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### Annexure-I

#### Application Form for the Position of JRF under the C2S Programme

(MeitY/3080449/03.05.2023)

Application for the post of .....

#### A. Personal Details:

1.	Name (in block letters):		Attach a Passport size Photograph
2.	Father's Name:		
3.	Date of Birth:		
4.	Gender:		
5.	Email Address:		
6.	Marital Status (Single /Married)		
7.	Contact Number (s):		
8.	Address for correspondence:		
9.	Permanent Address:		
10.	Category (Gen./OBC/SC/ST):		

<b>11.</b>	<b>Aadhar Number</b>	
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**B. Educational Details:**

Degree	Subjects	University/Institution	Year of passing	Grade or % of marks
10 <sup>th</sup>				
12 <sup>th</sup>				
BE/BTech				
ME/MTech				
Other				

**C. Experience Details (Teaching/ Industry/ Research)**

(In reverse Chronological order i.e. starting with latest experience first)

S. No.	Organization	Designation	Nature of Work	Duration	Salary

**D. Details of GATE/NET Qualification**

<b>Qualification Year</b>	
<b>Discipline</b>	
<b>Score</b>	
<b>Rank</b>	
<b>Marks Obtained</b>	
<b>Validity</b>	

### E. Other Details

<b>Details of Professional Skills</b>	
<b>Title of project dissertation</b>	
<b>How the above position is helpful in meeting your career goal (Max 250 words)</b>	Attach a separate sheet
<b>Details of Research Publications (If any)</b>	Attach a separate sheet
<b>Any other relevant information</b>	
<b>References (Two)</b>  (Name of two referees who are familiar with your academic and research background)	<b>1.</b> _____  <b>2.</b> _____

### DECLARATION

I hereby declare that the above information is correct to the best of my knowledge and belief. I understand that my candidature will be cancelled if any information is found incorrect at any given period of time.

**(Signature of the applicant)**

**Date:**

**Name of the Candidate:**

**Place:**

**Note:**

1. Original Certificate with one copy to be brought at the time of Interview only.